A 0.25-μm 20-dBm 2.4-GHz CMOS Power Amplifier With an Integrated Diode Linearizer

Cheng-Chi Yen, *Student Member, IEEE*, and Huey-Ru Chuang

***Abstract*—A 2.4-GHz CMOS power amplifier (PA) with an output power 20 dBm using 0.25-μm 1P5M standard CMOS process is presented. The PA uses an integrated diode connected NMOS transistor as the function of diode linearizer. It is believed that this is firstly reported to use the diode linearization technique in CMOS PA design. It shows effectively improvement in linearity from gain compression and ACPR measured results. Measurements are performed by using a FR-4 PCB test fixture. The fabricated power amplifier exhibits an output power of 20 dBm and a power-added efficiency as high as 28%. The obtained PA performances demonstrate the standard CMOS process potentialities for medium power RF amplification at 2.4 GHz wireless communication band.**

***Index Terms*—2.4 GHz, 0.25 mm, CMOS, diode linearizer, power amplifier (PA), WLAN.**

I. Introduction

DUE TO the fast development of wireless communication, the low cost, high performance and high integration technology is need for system-on-a-chip (SOC) implementation. The CMOS technology provides a good solution for SOC integration. Recent speed improvements of standard CMOS process makes it possible to implement RF blocks, such as low noise amplifiers (LNAs), voltage-controlled oscillators (VCOs) and mixers, for operating toward 5 GHz. However, the CMOS PA remains to be one of the most severe blocks due to the limited breakdown voltage, especially in advance submicron CMOS process. It is a very challenging task to implement a high performance CMOS power amplifier (PA).

For the improvement of the PA linearity, some linearization techniques such as feedforward, feedback, and predistortion have been developed, but they are not capable to be integrated in a single IC. Due to its small size and no extra dc current consumption, the diode linearizer [1], [2] is a good choice to be integrated in the PA design. The integrated diode linearizer in HBT PA can effectively improve the gain compression and phase distortion performances. In [3], a similar technique by using nonlinear capacitance cancellation in CMOS PA design has been reported. The integrated diode linearizer in HBT PA can effectively improve the gain compression and phase distortion performances by compensating the effects suffered from the gate dc bias level (V_{gs}) which decreases as the input power increases. A demonstration is shown as follows. A PA uses an integrated diode connected NMOS transistor as the function of diode linearizer is shown in Fig. 1(a). A time domain simulation of a 320-μm wide common source NMOS transistor without and with linearizer drives by input power from $-10\sim6$ dBm (biased with $V_{gs} = 0.8$ V) is performed by using the Agilent ADS. The simulated results show that, while the gate bias dc level of the transistor without linearizer drops to 0.71 V at input power = 6 dBm, that with linearizer has almost no change and maintains at 0.8 V. This shows how the diode linearizes the circuit. By using this technique, this paper presents the design of a 2.4-GHz CMOS PA fabricated in TSMC 0.25-μm 1P5M standard CMOS process with the integrated diode linearizer.

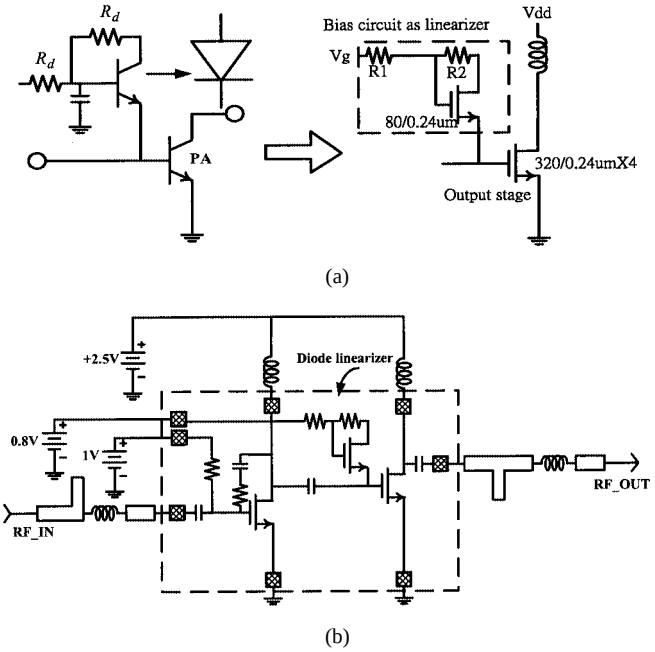

Fig. 1. (a) Schematic of the diode linearizer in PA. (b) Circuit schematic of a 2.4 GHz CMOS PA.

II. Circuit Design

In standard 0.25-μm 1P5M CMOS process, the NMOS transistor has a drain–source breakdown voltage about 5.4 V and a knee voltage about 0.5 V. With the limited 2.5 V drain dc supply voltage and poor power handling capability, designers face the severe challenge in designing the CMOS power amplifier. To reach high output power above 20 dBm, designers must use large size NMOS transistor to implement a PA, although it

Manuscript received April 4, 2002; revised July 30, 2002. This work was supported by the National Science Council, Taiwan, R.O.C., under Grant NSC 90-2213-E-006-055. The review of this letter was arranged by Associate Editor Dr. Arvind Sharma.

The authors are with the Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan, R.O.C (e-mail: chuangh@ee.ncku.edu.tw).

Digital Object Identifier 10.1109/LMWC.2003.808722

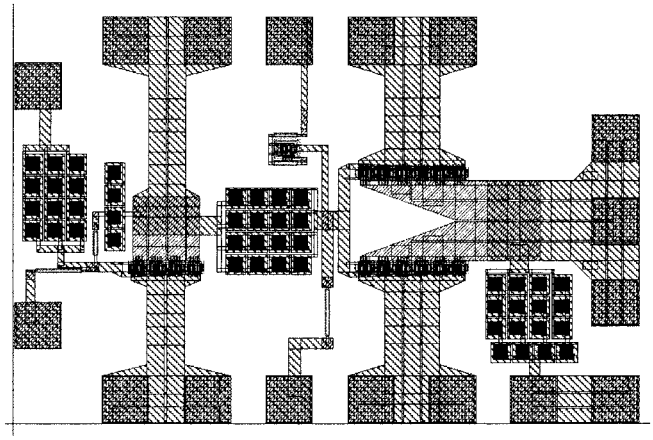

Fig. 2. Layout of a 2.4-GHz CMOS PA with a chip area of 1100 × 700 μm^2 including bonding pads.

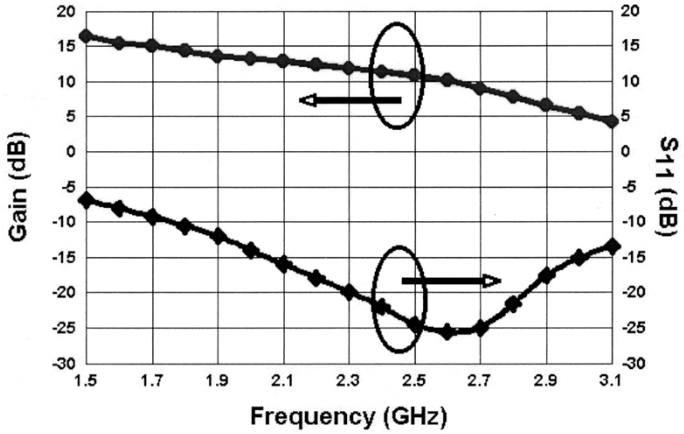

Fig. 3. Measured small signal gain and input return loss of the PA.

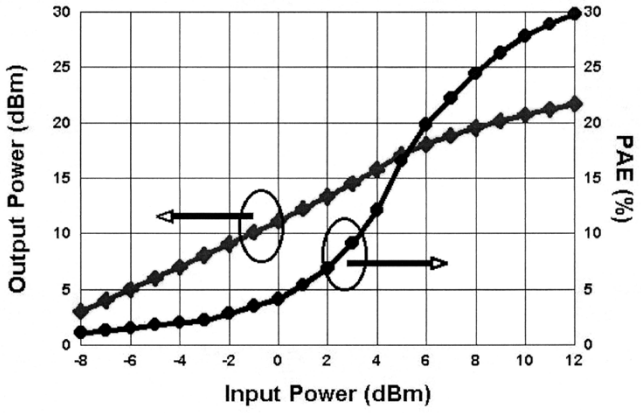

Fig. 4. Measured output power and PAE with the diode linearizer at 2.45 GHz.

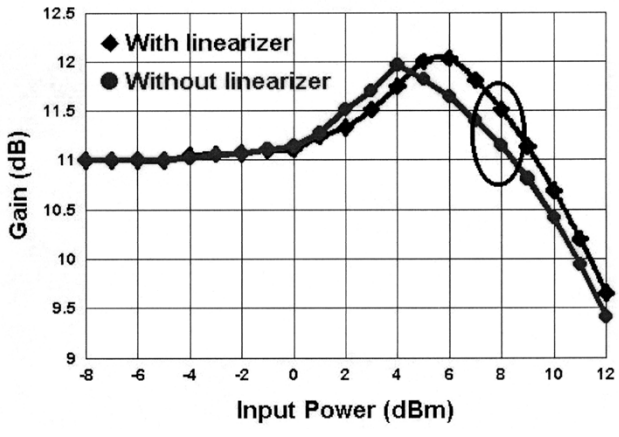

Fig. 5. Measurement of the gain compression of the PA at 2.45 GHz.

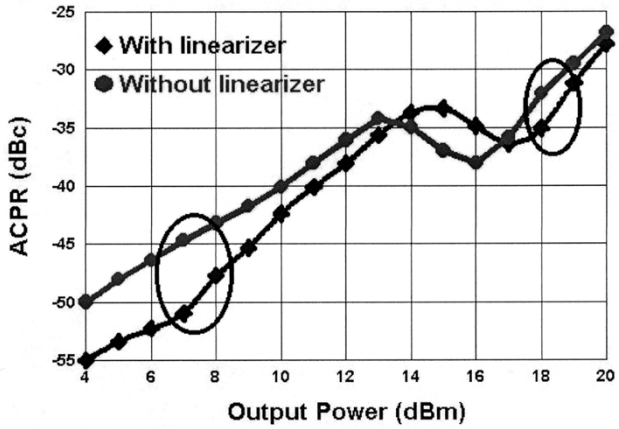

Fig. 6. Measurement of the ACPR measurement of the PA with $\pi/4$ DQPSK modulation at 2.45 GHz.

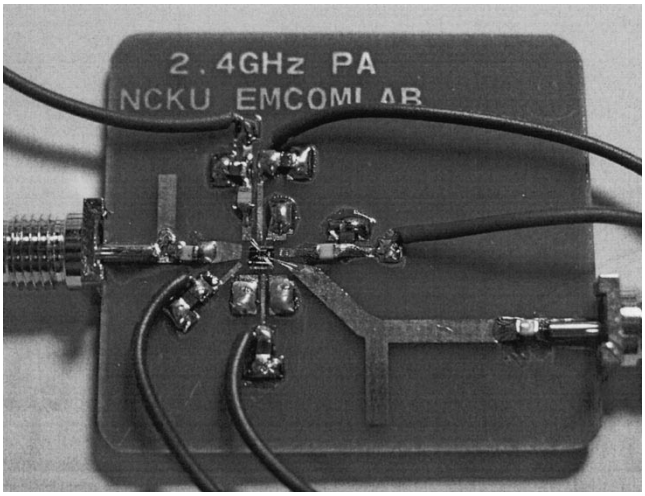

Fig. 7. Photograph of the PA on a FR-4 PCB test fixture.

will decrease frequency response due to the increase of parasitics. Fig. 1(b) shows the schematic of the two-stage PA. The output stage operates in class AB (near class B) to obtain high efficiency and the output transistor is 960-μm wide. The input stage operates in class AB to offer enough power gain and the size of the input transistor is chosen to be 1/3 of output transistor's size. Because the spiral inductors of metal-5 offered by the foundry are 10-μm wide and cannot carry high current density, both of the RF chokes are placed off-chip. The diode linearizer is formed by 80-μm wide diode connected NMOS transistor and is placed at the output stage as the gate biasing circuit. To avoid the loss of model accuracy, parts of the input and output matching networks are placed off-chip. But some matching information is kept in mind in simulation including the effects of FR-4 PCB test fixture and passive components. After

TABLE I
SUMMARY OF THE MEASURED CHARACTERISTICS OF A LINEARIZED 2.4 GHz CMOS POWER AMPLIFIER

Linearized 0.25-μm 2.4 GHz CMOS PA	
Operation Voltage	2.5V
Frequency	2.45GHz
Small Signal Power Gain	11.2dB
Input Return Loss	24dB
Output P_{1dB}	20dBm
PAE	28%
ACPR*	-28dBc@main channel power = 18 dBm
EVM *	2.2 %@main channel power = 18 dBm
Die Area	1100 x 700 μm^2

final tuning of the input and output matching network using microstrip line, the fabricated CMOS PA shows satisfactory performance in power gain and output power characteristics. Due to the large size of output stage transistor, it is partitioned into two separate parts and placed opposite. Fig. 2 shows the layout of the two-stage PA. The whole chip area is 1100 $\times$ 700 μm^2, including bonding pads.

III. MEASURED RESULTS

The measurement is performed on a FR-4 PCB test fixture. The PA chip is connected to the PCB test board by aluminum bond-wire. The equivalent model of the bond-wire is about 1 nH/mm. The measured small signal gain is 11.2 dB and input return loss is 24 dB at 2.45 GHz, as shown in Fig. 3. Fig. 4 shows the measured output power and power-added efficiency (PAE) of the PA using linearizer. It exhibits an output power of 20 dBm and a PAE as high as 28%. To compare the biasing topologies in linearity characteristics fairly, the two biasing circuits are integrated in the same PA chip layout but work individually, such that two biasing circuits can share the same FR-4 PCB test fixture. Fig. 5 shows the measured gain compression. The gain compression of the PA using diode linearizer is a little higher than that using conventional biasing topology. Fig. 6 shows the ACPR measurement of the PA with $\pi/4$ DQPSK modulation (data rate = 48.6 Kbps, channel spacing = 30 KHz, channel BW = 24.5 KHz). In most of the output power level, the measured ACPR of the PA with diode linearizer is better than that with conventional biasing topology. Fig. 7 shows the photograph the PA on a FR-4 PCB test fixture. Table I summarizes the measured characteristics of a linearized 2.4-GHz CMOS PA.

IV. CONCLUSION

A first-reported 2.4 GHz CMOS PA integrated with diode linearizer fabricated in the TSMC 0.25-μm standard CMOS process is presented. It is believed that this is first time to use the diode linearization technique in CMOS PA design. The integrated diode connected NMOS transistor serves as the function of diode linearizer can effectively improves the linearity of the fabricated class AB output stage without increasing chip size. The designed PA reaches an output power of 20 dBm and a PAE of 28%. It demonstrates the great potential of standard CMOS process in designing and manufacturing for 2.4-GHz PA.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC) of the National Science Council, Taiwan, R.O.C., for supporting the TSMC CMOS process.

REFERENCES

[1] T. Yoshimasu, M. Akagi, N. Tanba, and S. Hara, "An HBT MMIC power amplifier with an integrated diode linearizer for low-voltage portable phone applications," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1290–1296, Sept. 1998.

[2] ——, "A low distortion and high efficiency HBT MMIC power amplifier with a novel linearization technique for $\pi/4$ DQPSK modulation," in *IEEE GaAs IC Symp. Tech. Dig.*, 1997, pp. 45–48.

[3] C. Wang, L.-E. Larson, and P.-M. Asbeck, "A nonlinear capacitance cancellation technique and its application to a CMOS class AB power amplifier," in *IEEE RFIC Symp. Dig.*, 2001, pp. 39–42.